What is claimed is:

1. A sine wave generation circuit for stepwisely changing a voltage level of output in synchronization with an input clock signal to generate a pseudo sine wave, comprising:

a pulse generation circuit for generating a plurality of pulse signals using said clock signal as a reference; and

a voltage output circuit having a plurality of coefficient generation circuits for generating a plurality of different coefficients in response to the combination of bit information in said plurality of pulse signals and stepwisely changing the voltage level of said output in response to a coefficient series obtained when further combining the generated plurality of coefficients,

said plurality of coefficient generation circuits provided in said voltage output circuit and generating said plurality of coefficients including odd number generation circuits for generating odd number values of at least ternary-values inculuding coefficients on a positive side and coefficients on a negative side arranged symmetrically about a center coefficient.

2. A sine wave generation circuit as set forth in claim 1, wherein when the number of the coefficient generation circuits is n (n is a natural number of 2 or

more), at least (n-1) number of ternary-value generation circuits are included in the n number of coefficient generation circuits.

3. A sine wave generation circuit as set forth in claim 2, wherein said plurality of coefficient generation circuits comprise:

one binary-value generation circuit for alternately outputting a positive value and a negative value under the control of said pulse signals; and

(n-1) number of ternary-value generation circuits for repeatedly outputting a reference value and values at the positive side and values at the negative side from the reference value under the control of said pulse signals, and

wherein bit change points of the plurality of pulse signals output from said pulse generation circuit are defined so that the result of sampling at 2n number of equidistant points not including the maximum value, minimum value, and center point between them in a half cycle period from one of the maximum value and minimum value of the sine wave passing through the voltage change points of the pseudo sine wave to the other becomes said pseudo sine wave.

4. A sine wave generation circuit as set forth in claim 1, wherein:

said plurality of coefficient generation circuits have n number of ternary-value generation circuits repeatedly outputting a reference value and values at the positive side and values at the negative side from the reference value under the control of said pulse signals, and

bit change points of the plurality of pulse signals output from said pulse generation circuit are defined so that the result of sampling at 2n number of equidistant points including the maximum value or minimum value and a center point between them in a half cycle period from one of the maximum value and minimum value of the sine wave passing through the voltage change points of the pseudo sine wave to the other becomes said pseudo sine wave.

5. A sine wave generation circuit as set forth in claim 2, wherein

said plurality of coefficient generation circuits have n number of ternary-value generation circuits repeatedly outputting a reference value and values at the positive side and values at the negative side from the reference value under the control of said pulse signals, and

bit change points of the plurality of pulse signals output from said pulse generation circuit are

defined so that the result of sampling at 2n+1 number of equidistant points including the maximum value, minimum value, and center point between them in a half cycle period from one of the maximum value and minimum value of the sine wave passing through the voltage change points of the pseudo sine wave to the other becomes said pseudo sine wave.

6. A sine wave generation circuit as set forth in claim 1, wherein said plurality of coefficient generation circuits comprise

one binary-value generation circuit for alternately outputting a positive value and a negative value under the control of said pulse signals; and

(n-1) number of ternary-value generation circuits for repeatedly outputting a reference value and values at the positive side and values at the negative side from the reference value under the control of said pulse signals, and

wherein bit change points of the plurality of pulse signals output from said pulse generation circuit are defined so that the result of sampling at 2n-1 number of equidistant points including one of the maximum value and minimum value and not including the center point between them in a half cycle period from one of the maximum value and minimum value of the sine wave passing

through the voltage change points of the pseudo sine wave to the other becomes said pseudo sine wave.

7. A sine wave generation circuit as set forth in claim 1, wherein said pulse generation circuit is a shift circuit for shifting said input clock signal by exactly a predetermined time, wherein said plurality of coefficient generation circuits comprise:

one binary generation circuit for alternately outputting a positive value and a negative value under the control of said pulse signals; and

(n-1) number of ternary-value generation circuits for repeatedly outputting a reference value and values at the positive side and values at the negative side from the reference value based on a clock signal delayed in phase by exactly said predetermined time from said clock signal generated by said shift circuit and a clock signal advanced in phase by exactly said predetermined time; and

wherein said voltage output circuit generates said pseudo sine wave by adding the binary-value pulse signal output from said binary-value generation circuit and the ternary-value pulse signals output from said ternary-value generation circuits.